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[Letterhead of TER MEER STEINMEISTER & PARTNERS, European patent attorneys in Munich]

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Opposition against European patent 0 525 068
European patent application No. 91 908 374.1
Patent holder: Rambus Inc.
Opposer OIII: Hynix Semiconductor (Deutschland) GmbH

I.

We respond in brief to the main aspects in the submissions of the plaintiff dated August 12, 2002, relating to the impermissible widening of claims:

The latest observations by the patent holder bear witness to its lack of arguments. The only basis for disclosure that the patent holder can perceive in respect of claim 1 is in claim 103 of the original application, whereby it is striking that the patent holder cannot refer to a single passage in the description in support of its viewpoint. The patent holder is now laboriously endeavoring, by means of a "systematic interpretation" involving a comparison of claims 82, 95 and 97, on the one hand, and claim 103, on the other, to show that different bus architectures are addressed in the two groups of claims. In the following, we briefly comment on the flawed thinking that leads the patent holder to the latter conclusion:

1. The term "... capable of use" does not positively define any structural element of the claimed semiconductor device. (bottom of page 2 of the patent holder's submissions dated Aug. 12, 2002)

On page 19 ff. of our submissions of Aug. 12, 2002, we already showed that an evitable consequence of M1 (bus lines carry substantially all address, data and control information), M2 (bus has fewer lines than the number of bits in a single address), M3 (connection means of the semiconductor memory device is adapted to the bus according to the invention) and M4 (access-time register is "accessible to said bus through connection means") is that the

bus according to the invention is inevitably subjected to very specific spatial and physical adaptation.

2. At the top of page 3 of its submissions, the patent holder points out that the reference to "capable of use" in the bus architecture according to the invention does not exclude that the device can be deployed in a different kind of bus architecture.

By making this statement, the patent holder shows it is NOT questioning the fact that adaptation of the device according to claim 103 to a bus as described in the invention is an imperative requirement. Moreover, the entire content of the disclosures in the description of the invention establishes a close technical connection between the bus according to the invention and the access-time register, which is part of the device according to claim 103.

3. It is correct that a bus with particular properties and characteristics is discussed in the description of the present application. But these parts of the description are simply unrelated to the subject-matter of claim 103; the original application discloses many inventions (in the US 41 the patent (!) based on the corresponding application have issued). (middle of page 3 of the submissions)

All claims must be read in light of the description. In said description, under SUMMARY OF INVENTION, it is stated that:

The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected in parallel to a bus, where the bus includes a plurality of bus lines for carrying substantiated all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantiated fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

It is evident from this and from numerous other passages that a single basic inventive idea, namely the novel bus architecture, can be derived from the entire disclosures. Said bus architecture functions with

- semiconductor devices and

- memory devices

that are designed to work with it.

The independent claims relate to the system as a whole and to specific devices within the overall system. For example,

- claim 1 relates to "a memory subsystem",

- claim 13 to "a semiconductor subsystem bus",

- claim 82 to "a DRAM device",

- claim 95 to "a semiconductor device" with "at least one modifiable identification register",

- claim 97 to "a semiconductor device" with "at least one modifiable register to hold device address data bit" and

- claim 103 to "a semiconductor device" with "at least one modifiable access time register".

If reference is being made here to different inventions, then these can only be different devices, all of which being based, however, on the one, single, basic inventive idea of the new bus architecture. The reference to proceedings in the US is irrelevant, and misleading in its selectiveness (no mention of prosecution for fraud and the refusal to understand the bus feature as being unspecific, in Virginia).

4. At the bottom of page 3 and the top of page 4, the patent holder makes the point that the features

- said control information including semiconductor device-select information

and

- said bus carrying device-select information without the need for separate device-select lines connected directly to individual semiconductor devices

are contained in claims 82, 95 and 97, which relate to DRAMs, but not in claim 103, whereby the patent holder maintains that it was intentionally left open in claim 103 whether separate "device-select lines" are necessary.

The opposed patent refers repeatedly to three categories of information, namely

- address,
- data and
- control information.

Data and address information are unambiguously defined. The same applies to control information, which, as every person skilled in the art knows, includes all other types of information. It follows from this that device-select information will also be subsumed under control information by the person skilled in the art. This is also confirmed explicitly by the patent holder under SUMMARY OF INVENTION in the original application.

For this reason, a separate device-select line in excluded in claim 103 by virtue of feature M1 (the bus lines carry substantially all address, data and control information). The only qualification contained in feature M1 - the word "substantially" - clearly relates, according to the description, only to the aspect that special reset-in lines are provided for initializing a device according to the invention.

It follows from this that the two features mentioned by the patent holder that are included in claims 82, 95 and 97 but not in claim 103, are of clarifying nature only. The entire content of the description in the original application contradicts the assertion that said features were intentionally left out of claim 103.

The assertion made by the patent holder is based on the premise that features M1 - M4 do not exclude a separate device-select line. Such a statement is obviously false.

5. On page 4, the patent holder claims that its intentionally leaving open whether separate device-select lines are necessary, as it alleges, is logical "since the concept of the modifiable access-time register is in no way dependent upon separate inventions concerned with the particular features and protocol of the bus."

The patent holder fails to realize that the alleged basis of disclosure for claim 103 that is of relevance here pertains to a semiconductor memory device with a certain register and NOT a "concept of the modifiable access-time register". Both in claim 103 and in the entire description, the access-time register is exclusively an auxiliary instrument for co-operation between the semiconductor memory device according to claim 103 and the special bus architecture according to the invention.

Neither in claim 103 nor in the description is there a clear, direct disclosure to the effect that the access-time register itself can be viewed as an invention, independently of the bus in the invention. This conclusion on the part of the opposer can be arrived at not only by carefully analyzing the actual disclosures in their entirety. In their totality, the following indices support the opposer's position with overwhelming force:

- The applicant itself, and/or its patent attorneys and their specialists, have not thought at any time that the access-time register could have any significance in isolation from the bus according to the invention (we refer to the extensive arguments put forward in the submissions by opposers I and IV, dated Aug. 12, 2002).

- The examiner of the patent application on the basis of which the contested patent was granted viewed the features of the inventive bus in claim 103 to be significant, as can be seen from Annex OIII/14.

- The judge in the Rambus versus Infineon infringement proceedings in Virginia rejected any interpretation of the bus features as non-specific features of the invention.

- The expert witness, Prof. Thiele, has explained with reference to the description of the opposed patent, which is largely identical to the original application, that semiconductor memory devices connected to a conventional bus architecture are not protected by the patent.

6. At the top of page 6, the patent holder bases its argument on Prof. Thiele having stated "that the function of the access-time register is not in any way dependent on the bus structure in which it might be used".

This reference to Prof. Thiele merely confirms the fact that, from today's perspective, it is possible to deploy access-time registers independently of the new bus architecture (if one views a CAS latency register as an access-time register - an aspect that shall not be discussed further at this juncture). Hence, the statement by the patent holder says nothing about whether claim 103 can be seen as a basis of disclosure for claim 1 as granted. The expertise by Prof. Thiele suggests indirectly that this is not the case, since, as already noted, Prof. Thiele can only find one reference to a bus according to the patent in the entire opposed patent.

7. At the bottom of page 6, the patent holder points out that "several different methods are disclosed in order to detect collisions on the bus, all of them being independent of the provision of the modifiable access-time register in the slaves".

According to claim 103 and the description, the sole function of the access-time register, and also the only technical function of it to be disclosed, consists in avoided data collisions (and not in discovering data collisions). A logical consequence of this is the imperative and close technical relationship between the access-time register and the new bus architecture. This is not called into question by referring to different methods of discovering collisions.

II.

With its response of August 12, 2002, the patent also submitted 11 alternative petitions, of which the independent claims 1 of alternative petitions 5 - 11 now contain the following additional feature:

> "wherein a portion of the memory array (1) is automatically precharged in response to the read request, without further instructions".

This feature is supposed to be identical to claim 17 of the patent as originally granted, which read as follows:

> "wherein a portion of the memory array (1) is automatically precharged after executing the read request".

A modification has thus been made, in that, according to the new claim being sought, precharging can also be carried out now before or while executing the read request, and without any further instructions being made.

The additional feature above is no longer novel. From the prior art, it is already known how precharging can be carried out in response to a read request, and without any additional instructions, both before and after memory access.

Documents OIII/16 (US 4,330,852 - Redwine et al.), OIII/17 (US 4,528,646 - Ochii et al.) and OIII/18 (US 4,845,677 - Chappell et al.) are submitted as corroboration. These are previously published documents. As a consequence of the extensive modification by the additional features compared to claim 17 as originally granted, documents OIII/16, OIII/17 and OIII/118 are not from too late a date (Art. 114 EPC).

According to column 3, lines 51 - 58 of document OIII/16, the bit lines are automatically charged, specifically to a "full logic level". This is effected by clock signal ΦS after receiving the read request and **before** memory access, as can be seen from Figure 2. Furthermore, precharging is performed before data are outputted. Reference in made in this regard to lines a, c, d and h of Figure 2. That precharging is effected "without further instructions" is evident from the fact that no further signals are externally provided to the clock generator and control block 30.

Document OIII/17 discloses precharging **at the start** of a memory access, as can be seen from column 3 in lines 42 - 58. The Chip Enable Signal can be viewed here as a read request.

Automatic precharging of part of a memory array in response to a read request and without further instructions is also known from document OIII/18. In this case, precharging is effected **after** a memory access that is carried out in response to a read request. Figure 2 shows a block diagram for a 256K SRAM, from which it can be seen that data output (from DOB) triggers a reset/precharge signal that is supplied to preceding blocks or elements of the data path in order to prepare said blocks or elements for the next memory access. This can be seen from column 4, lines 58 - 68. The principle can also be applied in so-called "pipeline DRAMs", as described in column 5, lines 40 - 61. The only difference relative to a DRAM is that the precharge time is longer, with the result that subsequent accesses to the memory are performed in different sub-arrays to ensure that a subsequent access does not occur in one and the same array until the DRAM precharge time is over. Here as well, therefore, precharging is carried out in response to a read request without further external commands or control signals, in other words "without further instruction".

Peter Urner
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- Consolidation no. 6 -

Enclosures:
6 copies of these submissions
7 copies each of documents OIII/16, OIII/17 and OIII/18